However, the present embodiment uses the second epitaxial layer **100**A to form the active area **12** in order to prevent the formation of the cylindrical PN junction interface. The present embodiment also produces better homogeneity of the active area **12** to provide better electrical properties and more ideal criteria for IC design. In addition, because the field oxide layer **22** is replaced by the first trench **131**, the termination structure according to the present embodiment changes its planar feature to a steric feature. It leads to not only the reduction of the area of the termination structure, but also the reduction of current leakage. Therefore, the device performance is improved.

The DMOS device and the termination structure shown in FIG. **2** are compared with those of the present embodiment. The dielectric oxide layer **53** and the TEOS oxide layer **54** act as the isolation layer **181** of the present embodiment. The dielectric oxide layer **53** is formed by depositing an oxide layer and further applying a blank-etching process without a lithographic process. The TEOS oxide layer **54** is formed by depositing an oxide layer, using a lithographic process to define, and further applying an etching process. Contrarily, in the present embodiment, the formation of the isolation layer **181** also needs a lithographic process and an etching process, but it uses only one deposition. Moreover, for the DMOS device and the termination structure shown in FIG. **2**, the polysilicon layer **20** and the dielectric oxide layer **53** are directly etched without a lithographic process. Therefore, to completely remove the undesired portion of the polysilicon layer **20** and the dielectric oxide layer **53**, the etching process is more difficult to achieve. The dimension of the termination structure is limited. Compared with the prior art, the etching process for the isolation layer **181** of the present embodiment is not as limited as the prior art. The isolation protection is sufficient for isolating the gate and the source metal contact layer.

Also referring to the DMOS device and the termination structure shown in FIG. **2**, the polysilicon sidewall **33** needs to connects with the gate. However, as shown in FIG. **4**F in accord with present embodiment, the corresponding second polysilicon layer **142** connects with the source **191**. Therefore, for the design of the present embodiment, the potential of the second polysilicon layer **142**, the P-type second epitaxial layer **10**A, and the gate oxide layer **110** is the same. It prevents electric field crowding near the first trench **131** in the second epitaxial layer **100**A.

In another embodiment, as shown in FIG. **7**, compared to the embodiment shown in FIG. **4**E, a one-step etching process is carried out by using the second epitaxial layer **100**A as an etching stop layer to form the contact windows **170** of the active area and the second trench **171**. Therefore, the amount of P-type dopants implanted afterward must neutralize the existing N+ regions so as to form a plurality of P+ regions **161**.

The above-described arrangements of apparatus and methods are merely illustrative of applications of the principles of this invention and many other embodiments and modifications may be made without departing from the spirit and scope of the invention as defined in the claims. For example, the shapes and sizes of the components that form the camera supporting device may be changed. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A trenched DMOS device having a termination structure, the trenched DMOS device comprising:

a silicon substrate of a first conductive type, having a first epitaxial layer of the first conductive type and a second epitaxial layer of a second conductive type formed thereon;

a DMOS trench, formed in the first epitaxial layer and the second epitaxial layer;

a first trench, formed in the first epitaxial layer and the second epitaxial layer disposed close to an edge of the second epitaxial layer, the first trench to be utilized as a main portion of the termination structure having a bottom disposed in the first epitaxial layer;

a second trench disposed between the DMOS trench and the first trench, the second trench having another bottom disposed in the second epitaxial layer adjacent to a region of the second conductive type;

a gate oxide layer on the DMOS trench and the first trench, the gate oxide layer having extended portions covering an upper surface of the second epitaxial layer adjacent the DMOS trench and of the second epitaxial layer adjacent the first trench;

a first polysilicon layer, formed in the DMOS trench;

a second polysilicon layer, formed over the gate oxide layer in the first trench, having another extended portion covering the upper surface of the second epitaxial layer adjacent the first trench, the second polysilicon layer having an opening to expose the gate oxide layer disposed at the bottom of the first trench to split the second polysilicon layer into two discrete parts;

an isolation layer, formed on the first polysilicon layer in the DMOS trench and extended portions of the gate oxide layer adjacent the DMOS trench, on the second polysilicon layer, and on the gate oxide layer over the second epitaxial layer at the bottom of the first trench, the isolation layer having a first contact window to expose the second polysilicon layer over the second epitaxial layer and a second contact window to expose the second trench; and

a source metal contact layer, formed over the isolation layer and filling both the first contact window and the second contact window, having a connection with a source of the DMOS device and further having an edge beside the first contact window.

2. The trenched DMOS device of claim **1**, wherein the isolation layer includes a plurality of body contact windows extending into the second epitaxial layer, and wherein the source metal contact layer is formed over the body contact windows.

3. The trenched DMOS device of claim **1**, further comprising a drain metal contact layer formed on a backside surface of the silicon substrate.

4. The trenched DMOS device of claim **1**, wherein the isolation layer comprises doped silicate glass.

5. The trenched DMOS device of claim **1**, wherein the source metal contact layer comprises a stack of Ti, TiN, and AlSiCu alloy.

6. The trenched DMOS device of claim **1**, wherein the first conductive type is an N type and the second conductive type is a P type.

7. The trenched DMOS device of claim **1**, wherein the first conductive type is a P type and the second conductive type is an N type.